# C1onfig

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Config** | **Name** | **Config** |
| AXI\_masters\_num | 2 ( EDP EPP ) | nff | off |
| AXIM\_width | 128 bit | real\_time\_trace | off |
| AXI\_slave\_num | 1 ( EDAP ) |  |  |
| AXIS\_width | 128 bit |  |  |
|  |  | non\_linear\_units | 32 |
| DTCM\_size | 128KB | qman\_num | 8 |
| PTCM\_size | 32KB |  |  |
| PCACHE\_size | 32KB | sflp | 4 |
|  |  | spu\_xtend | off |
| mem\_power\_gating | off | vflp | 4 |
| memory\_ecc | off | vpu\_xtend | off |

# Diagram

# Interface

## CevaXM4 interface

|  |  |  |  |
| --- | --- | --- | --- |
| **General** |  |  |  |
| ceva\_free\_clock | 1 | I | Root clock |
| ceva\_sys\_wdog\_clk | 1 | I | System watchdog clock synchronous to root clock |
| ceva\_epp\_wdog\_clk | 1 | I | EPP watchdog clock synchronous to root clock |
| ceva\_edp\_wdog\_clk | 1 | I | EDP watchdog clock synchronous to root clock |
| ceva\_iop\_wdog\_clk | 1 | I | IOP watchdog clock synchronous to root clock |
|  |  |  |  |
| ceva\_core\_rst\_n | 1 | I | Asynchronous reset for the Core, active low |
| ceva\_sys\_rst\_n | 1 | I | Asynchronous reset for the Core and MSS, active low |
| ceva\_global\_rst\_n | 1 | I | Asynchronous reset, active low |
| ceva\_ocem\_rst\_n | 1 | I | Asynchronous reset for the Core, active low |

* watchdog clock跟ceva\_free\_clock是同源时钟。
* global\_rst\_n：reset整个DSP（CORE, MSS, PSU, OCEM）
* sys\_rst\_n： reset CORE, MSS（daisy-chain JTAG）
* core\_rst\_n： reset CORE （boot）
* ocem\_rst\_n： reset OCEM

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| --- | --- | --- | --- |
| **Boot Sequence** |  |  |  |
| boot | 1 | I | Boot request signal.Should only be set during reset |

* Boot from PC 0x0
* Boot from external location
* 从外部地址(vector)启动，boot和vector需要在reset之后保持至少8个cycle.
* 利用PDMA preload程序，register PDTC的bit 29（PDSC）表示transfer完成

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| --- | --- | --- | --- |
| **Program Cache Invalidate** |  |  |  |
| mcache\_incalidate\_strap | 1 | I | Memory Cache Invalidate Strap |

* Reset后保持stable 8个cycle，用来invalidate PCACHE。（也可以软件自己做）

|  |  |  |  |
| --- | --- | --- | --- |
| **Operation Mode Support** |  |  |  |
| ext\_pv | 1 | I | External Permission Violation indication, set if violation occurs in the users system |
| ext\_vom | 2 | I | External Permission Violation operation mode |
| cevaxm4\_seq\_om\_r | 2 | O | Operation Mode |
| cevaxm4\_seq\_pi\_out\_r | 1 | O | Permission Interrupt Output |

* ext\_pv、ext\_vom：USER0和USER1，外部产生一个permission violation（脉冲）， ext\_pv采样进MODQ PV，ext\_vom采样进MODQ VOM。reset是被clear，可以软件（pop mov）改动。
* cevaxm4\_seq\_om\_r[1:0]：表示MODQ OM
* cevaxm4\_seq\_pi\_out\_r：ppv\_set采样

|  |  |  |  |
| --- | --- | --- | --- |
| **External Wait** |  |  |  |
| external\_wait | 1 | I | External wait request |

* 外部的input让CevaXM4 core进入wait状态
* ext\_wait → psu\_core\_wait → wait state

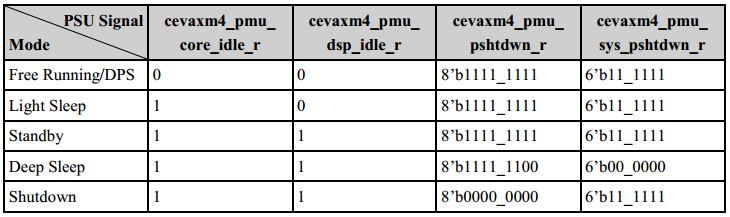
|  |  |  |  |
| --- | --- | --- | --- |
| **Gerneral Purpose Input/Output** | |  |  |
| gp\_in | 32 | I | General Purpose Inputs |
| cevaxm4\_gpout | 32 | O | General Purpose Outputs |

* 可以通过in/out {cpm}访问
* Register GPIN， 0x34， in
* Register GPOUT，0x38，out

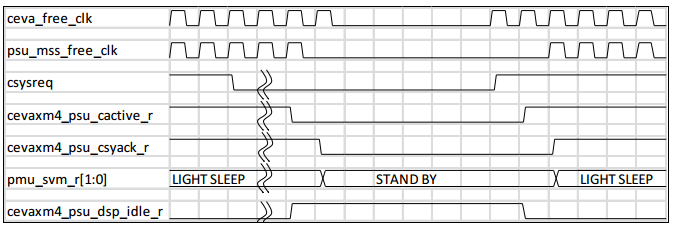
|  |  |  |  |
| --- | --- | --- | --- |
| **Verification Indications** |  |  |  |
| cevaxm4\_cverbit\_r | 1 | O | Verification error bit, set if a functional test fails. |
| cevaxm4\_seq\_eotbit\_r | 1 | O | End of Test bit, set when a functional test is finished. |

* 指令verifend，verifeq, verifeqs

|  |  |  |  |
| --- | --- | --- | --- |
| **PSU and AXI Low-Power Interface** | |  |  |
| csysreq | 1 | I | AXI Low Power Request to switch Light Sleep to Standby and vice versa |
| core\_rcvr | 1 | I | Recover from STAND BY/LIGHT SLEEP modes |
| stop\_sd | 1 | I | Stop core from shutdown. Restores the Core's power after Core is under power OFF state |
| cevaxm4\_psu\_cactive\_r | 1 | O | AXI Low Power Active indication |
| cevaxm4\_psu\_csysack\_r | 1 | O | AXI Low Power Acknowledge |
| cevaxm4\_psu\_rtck\_r | 1 | O | Return Test Clock(tck synchronized to ceva\_free\_clk) |
| cevaxm4\_psu\_dsp\_idle\_r | 1 | O | DSP Idle Indication (both clock and MSS clock can be turned off) |
| cevaxm4\_psu\_core\_idle\_r | 1 | O | CORE Idle Indication (Core clocks from PSU to core are shut down) |
| cevaxm4\_psu\_pshtdwn\_r | 8 | O | DSP Power Shutdown Request per unit domains{1core+MSS/1 Emulation/4 blocks of IDM/1 PTCM/1 pcache} |
| cevaxm4\_psu\_sys\_pshtdwn\_r | 6 | O | Memories retention mode-indication for Deep Sleep {4 blocks of IDM/1 PTCM/1 pcache} |



* psu指令写PSVM寄存器可以改变模式。
* 退出LS：int0/1/2，ext\_bp\_req1/2，vint，nmi，core\_rcvr
* Light Sleep和Standby互相切换



|  |  |  |  |
| --- | --- | --- | --- |
| **Multicore Messaging Interface** | |  |  |
| cevaxm4\_mcci\_mes\_int | 1 | O | Multicore Messaging Interface interrupt |
| cevaxm4\_mcci\_rd\_ind\_r | 32 | O | Multicore Messaging Interface read indication |
| cevaxm4\_snoop\_sn\_int | 1 | O | AXI Slave snoop interrupt |

|  |  |  |  |
| --- | --- | --- | --- |
| **Multicore Status Register Space** | |  |  |
| core\_id | 32 | I | Core ID identification |
| cevaxm4\_psu\_core\_wait\_r | 1 | O | Wait indication from the core |

* 利用AXI的独占式访问来实现外部共享memory的监控
* MCCI：consists of 32 command registers，write status and interrupt enable registers， and core status registers
* COM\_REG被写，则mes\_int拉高（COM\_INT\_EN有效），通过IO清掉；
* COM\_REG被读，则rd\_ind\_r拉高，拉高的cycle数由XCI\_COR(cpm0Xc60)决定
* core\_id：reset的时候被采样。可以被读取
* EDAP 0x400178
* IN 0x178
* OCEM chain 0x78
* Internal TCM Snooping：包含一个基址寄存器，一个top地址寄存器，一个控制和状态寄存器。中断通过IO去清。

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| --- | --- | --- | --- |
| **EDP AXI Capabilities** |  |  |  |
| cevaxm4\_psu\_mapv\_r | 1 | O | Access protection violation indication |
| acu\_lock | 1 | I | DACU and IACU lock indication. When asserted, the DSP and external masters cannot change the configuration of DACU and IACU |
| acu\_slv\_acc | 1 | I | When asserted, the external masters only can change the DACU/IACU configuration. When not asserted, the DSP only can change the DACU/IACU configuration (if the DSP is in supervisor mode). |

* 配置IACU/DACU寄存器，可以定哪些mode下哪些memory不能被访问，如果访问，则出mapv\_r中断。出了中断，DSP插入nop指令，直到nmi中断，所以在nmi中断处理程序里要解决violation，清掉中断，返回正确地址
* 相关寄存器：P\_MAPSR， P\_MAPAR， MAPSR， MAPAR

|  |  |  |  |
| --- | --- | --- | --- |
| **Semaphore Interface** |  |  |  |
| cevaxm4\_seq\_trp\_srv\_r | 1 | O | Trap service routine indication, set when the Core is in a trap |

* trap指令的子程序。
* trap：set； reti：reset

|  |  |  |  |
| --- | --- | --- | --- |
| **DMA Manager Interface** |  |  |  |
| qn\_desc\_en | 16 | I | QMAN enable descriptors increment signal |
| qman\_semaphore\_grant | 16 | I | QMAN semaphore grant |
| qman\_semaphore\_req | 16 | O | QMAN semaphore request |
| qman\_irq | 1 | O | QMAN violation indications interrupt |

|  |  |  |  |
| --- | --- | --- | --- |
| **Data DMA Indications** |  |  |  |
| next\_ddma | 1 | I | External control over DDMA Q(indication to progress to the next Q entry) |
| ext\_ddma\_dbg\_match\_ack | 1 | I | External Acknoeledge for DDMA debug match |
| cevaxm4\_ddma\_dbg\_match\_r | 1 | O | DDMA debug match indication |
| cevaxm4\_gvi\_r | 1 | O | General Violation Indication |

* 当QAUTO bit in MSS\_DDQS is set，DDMA在检测到next\_ddma（可以是异步的，但必须大于一个cycle）的上升沿时，启动一个transfer
* GVI中断，IO清，register DBG\_GEN（0xd14）[26:1]反应是什么问题

|  |  |  |  |
| --- | --- | --- | --- |
| **Interrupts Interface** |  |  |  |
| int0 | 1 | I | Maskable interrupt0 |
| int1 | 1 | I | Maskable interrupt1 |
| int2 | 1 | I | Maskable interrupt2 |
| nmi | 1 | I | Non-maskable interrupt |
| vint | 1 | I | Request signal for vector interrupt |
| vector | 32 | I | Address of the vector interrupt |
|  |  |  |  |
| cevaxm4\_uop\_int\_r | 1 | O | Undefined Opcode stretched interrupt |
|  |  |  |  |
| cevaxm4\_seq\_int0\_ack\_n\_r | 1 | O | int0 stretched acknowledge active low |
| cevaxm4\_seq\_int1\_ack\_n\_r | 1 | O | int1 stretched acknowledge active low |
| cevaxm4\_seq\_int2\_ack\_n\_r | 1 | O | int2 stretched acknowledge active low |
| cevaxm4\_seq\_int3\_ack\_n\_r | 1 | O | int3 stretched acknowledge active low |
| cevaxm4\_seq\_int4\_ack\_n\_r | 1 | O | int4 stretched acknowledge active low |
| cevaxm4\_seq\_bq\_ack\_n\_r | 1 | O | trape/breakpoint stretched acknowledge active low |
| cevaxm4\_seq\_nmi\_ack\_n\_r | 1 | O | nmi stretched acknowledge active low |
| cevaxm4\_seq\_vint\_ack\_n\_r | 1 | O | vint stretched acknowledge active low |
|  |  |  |  |
| cevaxm4\_epp\_wdog\_viol\_r | 1 | O | Indicates EPP Watchdog timeout |
| cevaxm5\_edp\_wdog\_viol\_r | 1 | O | Indicates EDP Watchdog timeout |
| cevaxm6\_iop\_wdog\_viol\_r | 1 | O | Indicates IOP Watchdog timeout |

# Synthesis Report

|  |  |  |
| --- | --- | --- |
| **Check List** | | **Bronze Netlist** |
| **Area (mm2)** | **Total (Cell Area)** | 2.48x4=9.92 |
| **Memory** | 0.588x4=2.352 |
| **Timing Result** | **ceva\_free\_clk** | 同源时钟  Period: 1.1 ns  Uncertainty: 0.1  Ps: slack=0.13，看了一下report，clock\_gating\_cell的setup=0.3影响比较大。 |
| **ceva\_edp\_wdog\_clk** |
| **ceva\_epp\_wdog\_clk** |
| **ceva\_sys\_wdog\_clk** |
| **ceva\_iop\_wdog\_clk** |
| **Library path** | | /LnxShare/yli/synopsys\_stdlib/db\_new/ssg/ts28nchslogl35hsh140f\_ssgwc0p81vn40c.db  /LnxShare/yli/synopsys\_stdlib/db\_new/ssg/ts28nchslogl35hsl140f\_ssgwc0p81vn40c.db  /LnxShare/yli/synopsys\_stdlib/db\_new/ssg/ts28nchllogl35hsl140f\_ssgwc0p81vn40c.db |
| **Memory path** | | /home/cliu/model/dc/mem/no\_pg/db/CEVAXM4\_RF\_1P\_128X21.db  /home/cliu/model/dc/mem/no\_pg/db/CEVAXM4\_RF\_1P\_256X32.db  /home/cliu/model/dc/mem/no\_pg/db/CEVAXM4\_RF\_1P\_1024X32.db  /home/cliu/model/dc/mem/no\_pg/db/CEVAXM4\_RF\_1P\_512X32.db |
| **Instance number** | | 1,629,171 x 4 = 6,516,684  Lvt: 5836 x 4 = 23344  Svt: 1623335 x 4 = 6493340 |
| **Percentage of LVT** | | %0.36 |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Module Name\* (in netlist)** | **Type** | **synopsys memory type** | **Word Num** | **Bit Num** | **Bit-write** | **Power gating** |
| CEVAXM4\_RF\_1P\_128X21 | HD RF (128K) | ts28nzh41p11sadrl128sa03p1 | 128 | 21 | FALSE | FALSE |
| CEVAXM4\_RF\_1P\_256X32 | HD RF (128K GEN2) | ts28nzh41p11sadgl128sa03 | 256 | 32 | FALSE | FALSE |
| CEVAXM4\_RF\_1P\_512X32 | UHD SRAM (2M GEN2 ) | ts28nzh41p11sad2l02msa05 | 512 | 32 | TRUE | FALSE |
| CEVAXM4\_RF\_1P\_1024X32 | UHD SRAM (2M) | ts28nzh41p11sadul02msa02p2 | 1024 | 32 | FALSE | FALSE |

# Verification Plan

# Register Space Allocation

* Registers（32bit） of CevaXM4 can be accessed by External Device through EDAP.
* Unused fields are marked as Reserved and must be written with a value of 0.
* EDAP receivers a 23-bit input address bus, which enables access of up to a 8MB memory space.

[22:21]==2’b00: IDM （128KB）

[22:21]==2’b01: PTCM（32KB）

[22:21]==2’b10: CPM register space

|  |  |
| --- | --- |
| Programming Model Sections | Address Mapping |
| MultiCore Configuration | 0x00400000 – 0x00400098 |
| OCEM | 0x00400104 – 0x0040017c |
| Wrapper | 0x00400180 – 0x004001ac |
| OCEM\_BPCOUNT\_DRD | 0x004001f0 – 0x004001fc |
| PROFILE | 0x00400300 – 0x0040037c |
| Program Memory Subsystem | 0x00400400 – 0x0040054c |
| Data Memory Subsystem | 0x00400614 – 0x0040064c |
| Error Correction Codes | 0x00400650 – 0x00400668 |
| Watchdog | 0x00400670 – 0x004006a4 |
| Interface Configuration | 0x00400700 – 0x00400928 |
| Undefined Opcode | 0x00400c58 – 0x00400c60 |
| Access Protection | 0x00400c80 – 0x00400c88 |
| DMA | 0x00400d04 – 0x00400d74 |
| Power Scaling Unit | 0x00400e50 – 0x00400e64 |
| Round Robin Arbiter | 0x00400fa0 – 0x00400fb0 |
| Queue Descriptor | 0x004010c0 – 0x004010d0 |
| Queue Manager Control | 0x004010dc – 0x004010f8 |
| Queue Manager | 0x00401100 – 0x004012f0 |

# Interrupt List

* CEVA中断ARM

|  |  |  |  |
| --- | --- | --- | --- |
| cevaxm4\_epp\_wdog\_viol\_r | 1 | O | Indicates EPP Watchdog timeout |
| cevaxm5\_edp\_wdog\_viol\_r | 1 | O | Indicates EDP Watchdog timeout |
| cevaxm6\_iop\_wdog\_viol\_r | 1 | O | Indicates IOP Watchdog timeout |
|  |  |  |  |
| cevaxm4\_gvi\_r | 1 | O | General Violation Indication |
|  |  |  |  |
| cevaxm4\_uop\_int\_r | 1 | O | Undefined Opcode stretched interrupt |
|  |  |  |  |
| cevaxm4\_psu\_mapv\_r | 1 | O | Access protection violation indication |
|  |  |  |  |
| cevaxm4\_seq\_trp\_srv\_r | 1 | O | Trap service routine indication, set when the Core is in a trap |
|  |  |  |  |
| cevaxm4\_cverbit\_r | 1 | O | Verification error bit, set if a functional test fails. |
| cevaxm4\_seq\_eotbit\_r | 1 | O | End of Test bit, set when a functional test is finished. |
|  |  |  |  |
| cevaxm4\_psu\_core\_wait\_r | 1 | O | Wait indication from the core |
|  |  |  |  |
| qman\_irq | 1 | O | QMAN violation indications interrupt |
|  |  |  |  |
| cevaxm4\_snoop\_sn\_int | 1 | O | AXI Slave snoop interrupt |
|  |  |  |  |
| cevaxm4\_mcci\_mes\_int | 1 | O | Multicore Messaging Interface interrupt |
| cevaxm4\_mcci\_rd\_ind\_r | 32 | O | Multicore Messaging Interface read indication |

# DDR Bandwidth Requirement